Meeting Nanometer Design Challenges

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Agenda

• Design Trend
• Nanometer Design Challenges
• Meeting The Challenges
• Conclusion
The Stakes Are Higher Than Ever
Risk on all sides

Time-to-volume risk: design in & demand

SoC development risk: >$25M & 1 year

Technology risk: partner dependencies

Cell libraries
Analog IP
Digital IP
Packaging
Foundry
Memory
Software
Processors
Testing
Internal development
There Is No Market for Second-to-Market

- **Mid-90s: Fast to Market**
  - 6 month late → ~31% earnings loss\(^1\)
- **Today: First-to-Market & First-to-Volume**
  - 3 months late = $500M loss\(^2\)
  - Product shipments ~1 yr.
  - Precise product windows

There are many design challenges !!
What’s Changing?

- Designs are getting bigger and more complex
- Signal Integrity affecting chip performance and functionality
- Low Power is critical
- 130nm is the fastest growing segment; and 90nm is on its way
- Design cost is climbing fast!
## Economics of SoC Development

<table>
<thead>
<tr>
<th>Category</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask Cost</td>
<td>&gt; $500K for 0.15um, &gt; $750K for 0.13um, and &gt; $1M for 0.1um</td>
</tr>
<tr>
<td>Development Time</td>
<td>9-18 months from feasibility to first sample</td>
</tr>
<tr>
<td></td>
<td>Successful projects typically require 3 tapeouts</td>
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<tr>
<td>Design Team</td>
<td>50 ~ 100: IC Design, System/Software, Test/Validation, Physical Design/CAD support</td>
</tr>
<tr>
<td>Total Development Cost</td>
<td>$10M ~ $20M USD</td>
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Interconnect Dominates Delay

The Cause

At nanometer geometries, coupling dominates wire loading

The Effect

Coupling Impact

Silicon respins
Longer design cycles
Lower performance
Lower yield
Wires Dominate Predictability

Wires drive iterations
- Pre-wire analysis is virtually meaningless
- Pre-wire optimization is virtually meaningless

Requires
- Wire-centric methodology
The Power Grid Problem

• IR drop
  – Voltage drops caused by current flowing through the resistive power network

• Ground bounce
  – Voltage spikes caused by current flowing from on-chip devices though the resistive ground network to the ground pins (or bumps)

• IR drop and ground bounce impact silicon performance
  – Increased clock skew → hold time violations
  – Increased signal skew → setup time violations
Signal Integrity Impact on Performance

Crosstalk increases delay

Crosstalk decreases delay
Impact of Crosstalk & IR Drop on Functionality

- Crosstalk glitches propagate to latches to create functional failures
- IR drop weakens victim driver, increases receiver sensitivity
- IR drop noise combines with crosstalk noise
Power Is Critical At 90nm And Below
No longer limited to consumer applications

Power Density Growth in Transistors*

Types of Power Concerns

• Dynamic power
  – Mainly due to charging/discharging parasitic capacitance – dictated by switching activity
  – Types of concerns:
    – Optimal battery life
    – System cost: sustained peak power dictates packages and cooling needs
    – System feasibility: short-term peak power effects on integrity/reliability

• Leakage power
  – Optimal battery life in standby mode
  – At 90nm, significant component of total power

• Power integrity
  – Ensure power supply infrastructure operates correctly and reliably in the target system

Source: Intel, 2004
SoC Verification
Massive digital & analog & software

Digital Gate Capacity

Over 70% of silicon re-spins contained functional errors

Analog’s Impact on Overall Design

SoCs with Digital and Analog

Transistors
Area
Effort
Re-spins

98%
80%
60%
50/50

2%
20%
40%
50/50

Digital
Analog
Nanometer Custom Design Issues
Integrating sensitive circuits with massive digital

Mixed-signal design
- Digital-analog co-verification
- Chip-level integration

Mixed-signal productivity
- Top-down methodology
- Layout, migration, & reuse

Foundry interface
- Accurate silicon modeling
- Process technology adoption
- Yield analysis & optimization
Delivering Complete SoC Verification
Cadence Incisive Platform

The industry’s most complete, well-integrated solution
How to Shorten Time to Tape Out?
Solve more of the problem earlier, faster

SoC Encounter – 1st full-chip interconnect
Traditional 1st full-chip interconnect

Get to final netlist
Get top-level plan
Block implementation

Quality logic
Top-level must be right
QoR: timing, SI, power, area, DRC clean / mfrg
Want fast TAT = productivity, time to tapeout
Big chips → want BIG blocks or else top-level unmanageable

RC First Encounter Nano Encounter

Better logic, predictable wires, faster run times = tape out sooner
Encounter Platform
High-performance architecture, best-in-class engines

OpenAccess Database
Encounter Platform
High-performance architecture, best-in-class engines

- Best synthesis – RC
- Best Virtual Prototype – FE
- New Global Physical Synthesis
- Best routing – Nanoroute
- Best SI – CeltIC
Encounter Platform

30-40 RTL- and netlist-to-GDS tapeouts at 90nm

- **North America**
  - 90nm 2.6M gate network processor chip tape-out Oct. 2003
  - 90nm 1.5M gate network processor chip tape-out Dec. 2003
  - 90nm 2.1M gate wireless application tape-out Nov. 2003
- **Japan**
  - 90nm 12M gate tape-out Jan. 2004
  - 90nm 3M gate consumer application tape-out Feb. 2004
  - STARC Starcad-21 90nm reference flow Mar. 2004
- **Europe**
  - 90nm 1.5M gate Bluetooth tape-out Dec. 2003
  - 3 more 90nm tape-outs scheduled for Q1/2004 + 7 more scheduled in Q2/Q3
  - Multiple 90nm test chips from multiple customers
- **Taiwan**
  - TSMC 5.0 90nm reference flow
Importance of Global Optimization

Old synthesis algorithms squeeze the best out of a local minima

New **Global** optimization finds the best overall structure => Higher Quality of Silicon

As design size increases, global synthesis optimization is critical!
Top-Level Planning – *Silicon Virtual Prototype*

- **RTL Synthesis**
- **Full-Chip Prototyping / Floorplanning**
- **Block-level Implementation**
- **Chip finishing + Signoff**

**Silicon Virtual Prototype**
- Placement
- Trial Route
- RC Extract
- Delay Calc
- STA
- Clock Tree
- IPO
- Power Plan
- Scan Opt.

**Complete “flat” physical design**
(proves timing and routability)

**VERY FAST!**

- Assess the logical design
- Guide the implementation
First Encounter vs Floor Planning

Typically save 6+ weeks in top-level planning

“80% market share”

_Dataquest, December 2003_
Block-Level Implementation

Why speed and capacity matter

- RTL Synthesis
- Full-Chip Prototyping / Floorplanning
- Block-level Implementation
- Chip finishing + Signoff

50MG using 2MG blocks
Top-level timing and SI closure difficult to impossible

50MG using 8MG blocks
Tractable top-level timing and SI closure

Customer Design
8MG, 130nm
Flat P+R, 32b Linux
Taped out March, 2004

Get to final netlist
Top-level plan
Block-level implementation
Block-Level Implementation – Fast Design Closure

- RTL Synthesis
- Full-Chip Prototyping / Floorplanning
- Block-level Implementation
- Chip finishing + Signoff

Global Physical Synthesis

Superthreaded Routing

Signal Integrity Closure
“Coarse pass”  “Fine pass”

Block-level Floorplan  Timing closure / Physical synthesis  Routing and SI  Post-route optimization  Signoff analysis

Design closure QoR – timing, SI, power, area, defect yield (w/ PDF Solutions)
New Nanoroute **Super Threading**
*Fast router gets faster*

- Applies Nanoroute multithreading over ordinary Ethernet
  - Very good results using groups of low cost 2-CPU desktop machines
  - Route 2M nets/hr, no special hardware

- Much more efficient than conventional distributed processing
  - Scales to large numbers of CPU’s
  - Easy to use

DAC 2004
13M gates, 3.3M nets
*Routed live in under 2 hours*
SI Closure Approach

Pass 1 – During Route (coarse pass)
- Wire spacing
- Layer switching
- Reduce parallel wires
- Net re-ordering

Pass 2 – Postroute Optimization (precision pass)
- Timing analysis
- Floorplan & partition
- Hierarchical CTS
- Power planning
- Signal Integrity analysis
- Global Physical Synthesis
- Extraction, Nanometer Routing
- Encounter platform
  High performance in-memory design image
- OpenAccess Database

"NanoRoute has reduced crosstalk errors by a factor of ten in the majority of our tape-outs."
- Deputy General Manager
  Major ASIC Vendor (Japan)
Integrated Sign-off Analysis

Built-in Sign-Off Analysis Engines

<table>
<thead>
<tr>
<th>Analysis Type</th>
<th>Engine</th>
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<tbody>
<tr>
<td>3D RC Extraction</td>
<td>Fire &amp; ICE QX</td>
</tr>
<tr>
<td>Voltage Drop Analysis</td>
<td>VoltageStorm</td>
</tr>
<tr>
<td>Delay Calculation</td>
<td>SignalStorm</td>
</tr>
<tr>
<td>Signal Integrity Analysis</td>
<td>CeltIC</td>
</tr>
<tr>
<td>STA</td>
<td>CTE</td>
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</table>

RTL/Gates → Prototype + Implementation
Power Management Techniques in Use

• System Architectural
  – Parallel architectures
  – Pipelining
  – Efficient data representation
  – Resynchronization for glitches

• Implementation
  – Multiple supply voltage (including on-off control)
  – Multi-Vt Optimization
  – Low power clocks
  – Back bias controls
  – Power spreading
  – Optimization, pin swapping, slew reduction
  – Cap cell insertion

• RTL Techniques
  – Efficient state representation
  – Clock gating
  – Operand isolation

• Circuit Techniques
  – Low Vt transistors
  – Cell Biasing
  – State keeper flip-flops
  – Memory power-down modes
  – Adiabatic control

• Layout/Process Technology
  – Long-channel devices
  – SOI
  – Multiple gate devices
  – High-K dielectric
Power is a Critical QoS Factor at \( \leq 90\text{nm} \) Can No Longer Be An Afterthought

Old multi-engine approach optimizes one axis at a time => Compromised results

Global approach enables multi-dimensional optimization => Optimal Quality of Silicon

Elaboration w/ clock gating
Tech independent optimization
Incremental optimization
Incremental opt with dual-vt

Area
Timing
Leakage
Switching

Elaboration w/ clock gating
Global structural optimization
Direct Target-guided optimization
Global focused tech mapping
Low Power Design Flow

- Low power synthesis
  - Clock gating, shutdown modes …

- Leakage power optimization
  - Multi Vt, optimization
  - State-retention power gating (SRPG)

- Multi-supply voltage design
  - Library/modeling
  - Physical synthesis/optimization
  - Clock tree
  - Power planning
  - Low-power clock design

- Automatic power grid generation

- Signoff power integrity analysis (VoltageStorm)

- Low-power synthesis / RTL clock gating
- Leakage (Multi-Vth) optimization
- Voltage-island-aware (Multi-Vdd) floorplanning + power planning
- Preliminary IR drop analysis
- Gate-level clock gating
- Placement + level shifter insertion
- Multi-Vth-aware physical optimization
- Low-power CTS
- Signal and power routing
- Post route Multi-Vth optimization
- Static IR-drop verification
- Dynamic IR-drop verification

Synthesis

Prototyping/
physical
planning

Physical
synthesis

Routing

Electrical
Verification
Low Power Design Flow
Collaboration with TSMC

TSMC and Cadence solve low power challenges at 90 nanometer and below with new TSMC Reference Flow

Cadence Encounter and Allegro Platforms Offer Comprehensive Power Closure and Packaging Solutions for Nanometer Design Using TSMC Reference Flow 5.0

SAN DIEGO, Calif. – June 7, 2004 – Cadence Design Systems, Inc. (NYSE:CDN) today announced the integration of the Cadence® Encounter® digital IC design platform and the Cadence® Allegro® system interconnect design platform, into TSMC’s Reference Flow 5.0, available today. This reference flow includes key Cadence technologies for low power design and chip-package design that enable higher productivity and improved design quality. This reference flow supports designs targeting TSMC’s 90-nanometer process technology. It is the latest milestone in the long-standing
Low Power Library Support
Collaboration with Artisan

Artisan and Cadence collaborate to optimize low-power chip design; new library views support next-generation low power devices

New Library Views Support Next-Generation Low Power Devices
Sunnyvale and San Jose, CA, October 4, 2004

Artisan Components (Nasdaq: ARTI) and Cadence Design Systems, Inc. (NYSE: CDN) today announced their collaboration to provide library views that enable designers to more effectively optimize low-power chip designs. The companies have partnered to create and qualify Artisan Library views based on the Cadence® effective current source model (ECOSM) format. These views provide customers with accurate delay prediction across a wide range of voltage levels and operating conditions using the Cadence Encounter™ digital IC design platform.
We Need To Brings It All Together

First to Market and First to Volume

State of the art tools
Proven Methodologies
Best Design Expertise